The Logic for High-Frequency ATE

ECLinPS-Plus is currently the world's fastest logic family. In the time it takes light to travel 1.7 inches, an ECLinPS-Plus device has completed a propagation delay (also known as a gate delay). The new family features flip-flop toggle frequencies of over 3 GHz, and propagation delays and rise and fall times as low as 100 ps. With this performance, automated test system designers can utilize the new logic ICs for optimal performance as frequency dividers, signal drivers over distance, and pico-second clock generators in leading edge high-frequency test systems.

"Have we hit the wall yet?" poses John Veto, Product Engineering Program Manager for Advanced ECL Products, ON Semiconductor. "Not quite. We're currently investigating advanced technology for next generation ECL devices that could cut propagation delays another 50% from the ECLinPS-Plus series.

The ECLinPS-Plus family includes nearly 80 devices, of which 23 are currently available and over 50 are scheduled to be released over the next year. Some of the new devices are direct pin-replacement upgrades to the existing ECLinPS-Lite logic family. In designing the drop-in upgrades, the company's project engineers were able to increase the speed and improve the timing performance without increasing the power. Thanks to tighter internal timing specifications, the new devices deliver advanced performance for systems that require high-speed clock distribution and data-synchronization.

Speed

The new ECLinPS-Plus devices are the world's fastest logic series, and customers have taken note. At LTX, Principal Engineer Steve Smith is part of a team dedicated to staying ahead of the leading edge in IC Test equipment. "In the cutting-edge environment of IC test, we are committed to using state of the art technology to meet the demanding performance requirements of our Fusion system-on-a-chip IC tester," says Smith. "We currently use a variety of ECLinPS-Lite components in our ATE designs. In our evaluation of the new ECLinPS-Plus components, their speed of over 3 GHz really impresses us, particularly since they operate at the same current levels as ECLinPS-Lite components."

Jitter & Propagation

"Another way to look at speed is in propagation delays," says Pete Weaver, Logic Portfolio Engineer at On Semiconductor. "Propagation delay of a line is important because unequal delays in parallel lines may cause timing errors. In long lines, the total delay time will often seriously affect system speed. Timing differences become increasingly important when designing clocks for high-speed flip-flops." The very first ECL devices exhibited gate delays of 1100 ps. The earlier generation ECLinPS-Lite series reduced gate delays to 300 ps. The new ECLinPS-Plus series cuts gate delays in one-third to 100 ps.

And the new devices deliver outstanding jitter performance. Weaver notes that, “Jitter is the variation in propagation delay from input to output. The low jitter capability of the ECLinPS-Plus series provides the unequalled signal stability and transmission reliability crucial for high-frequency test systems.”

Teradyne Hardware Design Engineer Dave O’Brien agrees. The Industrial/Consumer Division (ICD) of Teradyne, Inc. is the world's largest ATE manufacturer. “We produce instruments for testing high-speed digital communications devices such as ADSL systems, high definition TV, multimedia, and VDSL. We measured ECLinPS-Lite components for jitter, meaning the repeatability of the occurrence of edge placement relative to time. This measurement is one of the most important performance criteria for wide bandwidth applications. Our tests on these components revealed jitter of less than 0.5 ps rms. We're excited about the new design possibilities using ECLinPS-Plus because of its improved AC performance specifications."

Driving a Signal

A signal has three basic components, a rise and fall rate, amplitude, and the drive behind it. The edge of the signal, as it moves down a line, tends to degrade. “The challenge,” says Paul Shockman, Senior Applications Engineer at On Semiconductor, “is to keep a sharp edge. ECLinPS-Plus has some of the fastest edges in the world. One fast edge after another results in high speed transmission. Edges determine high speed transmission, while clock rates are actually a consequence of the edge rate.”

LTX’s Smith notes that “the faster rise and fall times available with the ECLinPS-Plus series lessen the effect of system noise. We need low jitter and high timing accuracy in our critical components to achieve our noise objectives.”

As an example, the new series MC10EP16 Differential Receiver delivers rise and fall times of 100 ps (min) to 200 ps (max) at 85 degrees C. When operating at 200ps rise and fall time, the device operates at a frequency of 2.7GHz. At 100ps, the device hits 3.4 GHz.

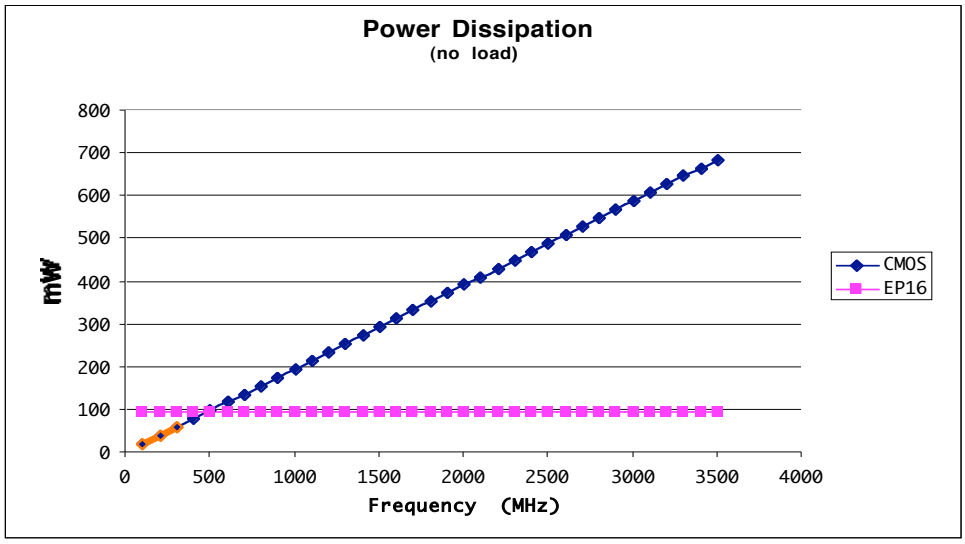
As the operating frequencies have increased from one generation of ECL family to the next, the specified amplitude has remained constant and become an industry standard at 800 mV. At 3.4 GHz, the upper edge of the operating envelope, the MC10EP16 boasts a 400 mV peak to peak amplitude and responds to input sensitivity down to a minimum of 150mV. At 1 GHz, the differential widens to 800 mV maximum amplitude while it still retains its input sensitivity of 150 mV.

The distance a device can drive a signal down a line depends in part on the quality of the medium, whether it be cable or circuit board. A simple rule applies: Better cables cut line loss. For long-distance driving over coaxial cable, the ECLinPS-Plus series features a special Coaxial Cable Driver, the MC10EP89. With maximum transmission amplitude of 1400 mV, it still responds to 150 mV signals and can drive a signal thousands of feet, even miles depending on cable quality. This device features preliminary edge rates of

230 ps rise and 210 ps fall @ 85° C with a 1.4V swing in amplitude, measured at maximum clock rate.

Power Dissipation (P_D)

By its very design, Bi-Polar ECL technology exhibits higher power dissipation compared to CMOS devices. Although CMOS performance continues to improve, power dissipation is beginning to become a major concern as operating frequencies increase. CMOS technology labors under a power dissipation formula that results in a significant increase in power dissipation with each linear increase in frequency. A big difference between ECL and CMOS technologies, according to Shockman, is that "as the frequency changes in the ECL power dissipation equation, the current stays the same. So there's no frequency scaling regardless of the device's speed. By contrast, as the frequency of a CMOS part increases, so does the power dissipation, thereby, increasing the possibility of device failure due to heat."



As CMOS device frequency capability increases, there is a point at which both CMOS and ECL devices will consume the same amount of power. Above this crossover point, ECL devices maintain relatively constant power dissipation and therefore high device reliability at higher frequencies. At frequencies above the crossover point, CMOS devices will face increasing power dissipation demands. "The crossover point may vary from device to device (ECL vs. CMOS), but it can be calculated for specific instances. As a general rule," Shockman notes, "you'd probably be safe placing the crossover point at approximately 500 MHz."

The termination power dissipation for ECLinPS-Plus devices, using 50 Ohms to Vtt, is typically 13 mW per output. The total power dissipation is the sum of the power dissipation of the chip plus the termination. Chip dissipation is fixed and constant over the frequency range per specification. For example, the MC10EP16 has a typical I_{EE} of

mA. Therefore, the chip P_D is 79 mW (24 mA x 3.3 V). Now add the termination dissipation of 13 mW, and the total power dissipation (P_D) totals 92 mW, even at 3.4 GHz.

The ECLinPS-Plus Family

The new ECL Plus family features five different types of devices: Buffer Chips, Signal Dividers/Clock Generation Chips, Translators, Line Drivers, and traditional Logic. LTX's Smith observes that "the comprehensive range of component sizes and packages available in the new ECLinPS-Plus series gives our design team more options for circuit design. The new broad range of low-profile packages gives us greater flexibility in designs where component height is a crucial factor."

"All devices that include 100EP in their part number," notes ON Semiconductor's Veto, "are both voltage and temperature compensated, whereas the 10EP designation denotes voltage compensation only. "

One of the most popular devices in the new family is the Programmable Delay Chip (Part # MC100EP195). This unique buffer chip performs two primary functions. First, it delivers a specified voltage to a specific pin and second, it can vary the propagation delay, crucial for instrument makers who require extremely precise timing for multiple lines. The device is programmable over a 10 ns range in 20 ps step resolution. The device effectively synchronizes edges at the end of the line.

Another popular chip, the MC10EP016 can divide a signal by any number between 2 and 256 at a frequency of 1.3 GHz with cascading capability.

The MC100EP139 Signal Divider/Clock Generation Chip divides the clock signal by 2/4 and also by 4/5/6. It generates two differential outputs for each of the two divider chains. The product family includes several other devices currently available with more signal dividers and clock generation chips scheduled to be released in the next year.

The ECLinPS-Plus family features a rich selection of basic logic chips that include devices such as the 4-input OR/NOR (MC10EP01), the 2-Input Differential AND/NAND (MC10EP05), the Differential 2-Input XOR/XNOR (MC10EP08), or the Dual Differential 2:1 Multiplexer (MC10EP56).

"The MC100EPT23 Dual Differential PECL to TTL Translator is the fastest translator available," says Veto. The family includes a wide selection of translators including all industry standard TTL or CMOS outputs.

In addition to the MC10EP16 and MC10EP89 Differential Line Drivers mentioned above, the ECLinPS-Plus line includes several additional line drivers, and more will be introduced next year.

For the most up to date information about available parts and specifications, please visit the ON Semiconductor website at: www.onsemi.com.

Summary
The new ECLinPS-Plus family of high-speed logic products offers rich opportunities for ATE manufacturers. The ATE community is already buzzing about the performance characteristics of the new series including higher speed, tighter jitter performance, faster edge rates, reduced system noise, and advanced line driving capabilities. And many of the new ECLinPS-Plus parts have been designed as direct pin replacement upgrades for their earlier ECLinPS-Lite counterparts.