The Worldwide Packetized Revolution

by

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Advanced developers and product engineers at leading communications and networking infrastructure companies are fomenting a worldwide revolution. In today's digital world, the networking and communications industry typically delivers separate voice, fax, and data modem services to customers. And today's communications infrastructure operates as separate real-time (circuit switched) and data (packet) using standard specific platforms that are, in many cases, based on proprietary technology.

The revolution in the communications industry is to a completely Packetized world. Already underway at leading chip makers and at the design teams of leading equipment providers, the revolution will be fully realized across the communications and networking industry within the next few years. The revolution to a Packetized world will overthrow the digital world by delivering unified services to customers. All services will be delivered in real-time over packet networks using common platforms based on open architectures.

"Why is the Packetized Revolution underway?" you might ask. Communications infrastructure providers are being driven by a seemingly never ending demand for higher capacity networks. These networks support ever increasing numbers of users, each of whom requires more and more bandwidth. New applications such as wireless Internet access, video services, and Voice over Internet Protocol (VoIP) are driving the demand for better audio, video, and data services.

Circuit switched systems provide excellent real-time services, but utilize bandwidth poorly. Even when a user is not talking, bandwidth is still used. Packet switched networks, by comparison, provide "bandwidth on demand". However, until recently, Packetized networks couldn't support real time services nor could they guarantee quality of service (QoS). Thanks to recent significant improvements, Packetized networks can now deliver acceptable QoS. This liberates communications network operators to support real-time services over unified packet networks.

One of the key enablers for the shift to Packetized networks will be new, advanced DSPs. DSP technology provides the required capability to "convert" real-time information (typically coming over a PCM highway) into Packetized data. The DSP will then send the Packetized data out over a Packetized network such as Ethernet or ATM. Critical enabling DSP functions include compression, echo cancellation, and packetization. All of these functions will be performed at the gateway. To do so effectively, the DSP must

be “network ready”, meaning that it’s able to link directly to both the PCM highway and the Packetized network. Up to now, such a device has not been available.

However, Motorola recently announced the new MSC8101 DSP. The MSC8101 is Motorola’s first product based on the SC140 DSP core introduced by the Star*Core Alliance. With four arithmetic-logic units (ALUs), the SC140 executes 1.2 billion DSP instructions per second at its initial clock speed of 300 MHz.

Product designers at Motorola surrounded the SC140 core with an unparalleled set of peripherals and capabilities that drive the MSC8101’s effective performance even higher. One of the most notable additions is the Communication Processor Module (CPM), an embedded RISC protocol-processing engine. The CPM enables direct connection to high-speed Packetized backbone networks in such protocols as ATM, Fast Ethernet, and PCM highways such as E1/T1 and E3/T3. The MSC8101 is the first DSP optimized for these networks and is, in fact, “network ready”. With this powerful set of enabling capabilities, the MSC8101 is leading the revolution away from circuit-switched systems to “convergent” packet-switched networks that deliver voice, data, fax, and modem services, all in real time. Let’s now take a brief look at some of the target markets and applications for the new device.

“Packetized” Markets

The Communications and Networking Market today accounts for 45% of the DSP market. The MSC8101 is targeted for communications equipment makers who meet the infrastructure needs of this market. Within this target market, the primary applications fall into five main categories: Wireless Infrastructure, IP Telephony, ATM Edge and Carrier Switches, Modem Banks, and WAN Switching and Transmission.

Wireless infrastructure includes basestations and switching devices for current second generation (2G) wireless and forthcoming 2.5 G and third generation (3G) applications. IP Telephony will require IP (Internet Protocol) gateways for voice, fax, modem, and video. Likewise, ATM Edge and Carrier Switch markets will require ATM gateways for voice, fax, modem, and video. Modem Bank applications include xDSL modems and Hybrid modem banks, while WAN Switching and Transmission require centralized DSP services such as compression and echo cancellation.

Let’s pause for a moment and consider the factors in the market place driving the development of the Packetized revolution. Perhaps the most pressing, urgent, and compelling market driver is that equipment manufacturers have reduced their design cycle times to remain competitive. Additionally, manufacturers are targeting high volume markets. To complete, they must slash the time between market launch and production volume ramp up.

To achieve faster time-to-market, equipment makers are seeking programmable DSPs that support multiple standards and multiple applications. Different software can differentiate applications on the same DSP. A DSP device that can be programmed in

higher level C and C++ languages facilitates rapid application development. Further, if the DSP is reprogrammable, equipment providers can ship subsequent ~~provide~~ software upgrades as standards evolve and new standards appear. Additional strategies for systems developers include better tools, reuse of hardware, and application software libraries. ~~Avner: Excellent! Just what I was looking for!~~

Other market drivers play a significant role. For unified packet networks to achieve widespread market acceptance, semiconductor manufacturers and systems developers must drive the cost per channel down. To meet this need, equipment manufacturers are employing system-on-a-chip (SoC) design methodologies to produce denser systems with higher integration. The resulting silicon devices can then interface directly to the Packetized network.

Architecture

Three major functional blocks combine in the System-on-a-Chip (SoC) configuration of the MSC8101. The "extended core" block runs at up to 300 MHz and includes the SC140 DSP core, the on-chip SRAM, the enhanced filter coprocessor (EFCOP), the HDI16 host interface, and the program interrupt controller. The second block, the CPM, contains the serial communications channels with the RISC communication processor and operates at 150 MHz. The third block, the system interface unit (SIU), supplies a circuit board's worth of system control and glue logic. The SIU includes interfaces to memory and to an external PowerPC bus and operates at up to 100 MHz.

Two phase-lock loops (PLLs) enable the multiple frequency scheme of the MSC8101. The PLLs enable each block to run at its optimal speed without wasting power. On-chip resources communicate via a 100 MHz, 64-bit internal PowerPC bus. The initial version of the MSC8101 operates at 1.5 volts internally, but provides standard 3.3-volt input/output to external components. (See Block Diagram of MSC8101).

The Star*Core Alliance

The Star*Core Alliance, a unique collaboration between Motorola and Lucent Technologies, was formed in 1998. The Alliance's purpose is to develop new, superior core architectures and development tools for future communications, transportation, and consumer electronics applications. While the Star*Core Alliance focuses on the fundamental DSP architecture, processing cores, and associated development tools, the two Star*Core partners are independently developing distinct chip products by combining these cores with their own peripherals, coprocessors and accelerators, memories, input/output devices, and system integration modules. Using the SC140 Core as a starting point, Motorola integrated it with a variety of peripherals and with PowerPC technology. The resulting Motorola MSC8101 is the first such chip based on the Star*Core architecture.

Process Technology

Motorola's high-end PowerPC process technology, called HiPerMOS-6 (HiP-6), enables the advanced performance and feature set found in the MSC8101. The HiP-6 state-of-the-art process technology features 0.13 micron sized features and advanced copper interconnects. The HiP6 process technology enables system developers to integrate various technologies on a single device. Available IP (Intellectual Property) in Motorola's extensive library includes the PowerPC bus interface, the MPC8260 Memory Controller, the MPC8260 CPM, and the FSRAM memory cell, which provides the MSC8101 with 512 KB of on-chip memory. All of these preceding IP modules are offered in the same compatible HiP-6 process technology.

The HiP-6 process technology that enables the MSC8101 results in a 17mm by 17mm plastic package, an exceptionally small footprint – particularly considering the large amount of memory and logic integrated on-chip. The chip's outstanding code density facilitates additional space savings. Outstanding code density enables the application to be encoded (programmed) in less space, thus more programs can be stored in the available internal memory space.

Performance & Performance Density

The result of the advanced integration and process technology offered in the MSC8101 is the industry's best performance density—i.e., the ratio of performance to power dissipation, board space, and system cost. Communication equipment manufacturers constantly seek the means to deliver greater channel-processing capacity while keeping costs and form factors to a minimum. The MSC8101 provides just the solution. Best-in-class development tools, some from leading third-party vendors, empower customers to develop advanced applications in rapid time-to-market design cycles, yet do so at the lowest cost per channel in the industry.

The SC140 processor core packs four data arithmetic-logic execution units (ALUs). Each one consists of a multiply-accumulate unit (MAC), a logic unit and a bit field unit (BFU), which serves as a barrel shifter. This architecture offers twice the number of MAC units available on previous DSP cores. Twice the MAC units provides customers with at least twice the performance for such crucial DSP tasks as finite pulse response and infinite impulse response (FIR and IIR) filters and fast Fourier transforms (FFTs). In addition to the four data execution units, the core contains two address arithmetic units (AAUs), one bit manipulation unit (BMU), and one branch unit. As a unit, the SC140 can issue and execute up to six instructions per clock – e.g., four independent arithmetic instructions and two pointer related instructions, such as moves or other operations on addresses.

The SC140 processor core is twice as powerful as other DSPs in its class. At its initial clock speed of 300 MHz, the SC140 can execute 1,200 DSP MIPS, meaning 1.2 billion multiply-accumulate operations, together with associated data movement functions and pointer updates each second (equivalent to 3000 RISC MIPS). In addition to this core performance, Motorola has added several other functional blocks that further enhance the MSC8101's performance. The EFCOP adds an additional 210 effective MIPS in functions such as echo cancellation (assuming 70 percent utilization of the coprocessor at 300 MHz). The CPM boosts performance further by providing a separate high-performance engine for low-level protocol processing. The MSC8101 features the highest external bandwidth of any DSP (6,400 Mbps), enabled by its 32-/64-bit, 100 MHz PowerPC bus interface. The on-chip zero-wait-state SRAM memory eliminates the penalty for off-chip memory accesses. The 16 channel DMA and program interrupt controller furnishes additional parallelism, off-loading the processor core.

Equipment manufacturers can expect the SC140 core to sustain this advanced performance over time due to the flexibility of its data execution units. The four data execution units can operate simultaneously in any combination. For example, the core could execute four multiply-accumulate operations in a single clock, or one MAC, two-arithmetic/logical operations, and one bit field operation. Because all four data ALUs are identical, the SC140 exhibits great flexibility in the assignment and execution of instructions. This leads to the increased likelihood that all four execution units will be in operation on any given cycle, so programs can better utilize the core's parallel architecture.

The MSC8101 delivers both the industry's highest performance and the best performance density. Low power consumption, small size, and integrated feature sets, many of which would normally require external components (memory, memory control logic, network connectivity devices, etc.), elevate the MSC8101 to the apex of performance density in the industry. The chip provides enough horsepower for an entire T1/E1 line's worth of channels (i.e., 24/30 channels), but draws only 0.5 W. The entire communications market for DSP devices demands performance density as a central requirement. Equipment manufacturers strive to pack the greatest possible channel-processing capacity in the smallest possible volume, and the lowest possible power consumption, all at the lowest price. By this crucial measure, the MSC8101 answers the market's demands in no uncertain terms.

Networking

Other DSPs stand a distant second when it comes to on-chip networking capabilities. The MSC8101 ships as the first "network ready" DSP. It comes with built-in protocol processing support for the latest network protocols. This enables equipment designers who use the MSC8101 to connect their equipment directly to Packetized backbones. The on-board CPM's serial communication channels include two fast communication controllers (FCCs) designed to handle the latest high-speed networking protocols.

All protocol processing is handled by microcode stored in the communications processor's (CPM) ROM and, if the user chooses, the CPM's RAM. The use of RAM-resident microcode allows customers to dynamically update the MSC8101's protocol algorithms. As new protocols or enhancements to meet the requirements of evolving standards and changing customer requirements become available, customers can stay abreast by simply updating their existing MSC810x series chip. The MSC8101 is the only DSP to offer such reprogrammability.

Protocols currently included are 100-Mbps Fast Ethernet, 155-Mbps ATM (Asynchronous Transfer Mode) SAR functions (including AAL 0, 1, 2, and 5), and HDLC up to T3/E3 rates (45 Mbps). Collectively the FCCs provide aggregate serial data rates of up to 510 Mbps, equivalent to one full-duplex ATM connection, two full-duplex Fast Ethernet connections, or a combination of one full-duplex ATM and one full-duplex Fast Ethernet connection.

The CPM includes a pair of multichannel communication controllers (MCCs) which support multichannel HDLC transmission used by T1/E1 lines, for example. Each of the two MCCs can handle up to 128 full-duplex serial channels, for a total of 256 64-Kbps channels. Two accompanying time-slot assigners (TSAs) enable these channels to be multiplexed on up to four time-division multiplexed (TDM) ports. Using the TDM ports, the MCCs support a total of four T1 or E1 lines.

The CPM also provides two full-duplex serial communication controllers (SCCs), two management controllers (SMCs), one serial peripheral interface (SPI), and an inter-integrated circuit (I^2C) interface. The SCCs support seven user-selectable protocol types: 10 Mbps Ethernet, HDLC/SDLC, HDLC Bus, UART/Synchronous UART, BiSync, LocalTalk, and Transparent Mode. The SMCs can perform framing and serial interface tasks in ISDN-type applications. They can also act as universal asynchronous receiver/transmitters (UARTs) or as transparent channels.

The CPM's various serial channels operate independently and provide bursting. Each can be assigned a different protocol at any given time. Each channel is accompanied by two on-chip microcoded serial direct memory access (SDMA) controllers, one for receiving and the other for transmitting.

The CPM operates separately from the core processor and performs several key functions. It transfers information, handles serial channel interrupts and performs built-in Layer 2 and Layer 3 protocol processing functions independently (Layer 1 functions are built into the hardware). This leaves the core free to handle high-level tasks. The CPM takes incoming frames of information, strips off headers, and extracts "payload" data. Only when the frame has been completely disassembled and payload data stored in memory, is the core interrupted. The CPM performs the same functions in reverse for outgoing information, assembling payload data into frames and transmitting it via the serial channels.

In today's systems, an MCU is connected to the network. In this centralized data flow, the MCU extracts the payload data from the stream by analyzing headers and frames. It then redistributes this payload data to the DSPs through the host port or serial ports. The problem: If each DSP processes 30 channels (E1 worth) and there are 24 DSPs connected to the MCU, the MCU will not be able to handle the traffic. In short, the MCU becomes the system bottleneck. With new distributed data flow systems, each of the MSC8101 DSPs in the system hook directly to the network. The CPM in each DSP then extracts payload data directly from the network. Please note that because of its flexible capabilities and onboard CPM, the MSC8101 can be used in either a centralized or distributed configuration. (See Data Flow chart.)

~~<I need some input about distributed data flow. Can you give me a raw material paragraph? I only have a one page diagram with no text. Help!)~~

~~Avner: I believe you refer to the block diagram that is in the press release slides, which shows the distributed versus centralized data flow. Today systems are using centralized data flow where the microcontroller (MCU) is connected to the network. The MCU (such as MPC860 and MPC8260) extracts the payload data from the stream by analyzing the headers and frames. Then it redistributes this payload data to the DSPs through the host port or serial ports.~~

~~As long as each DSP is processing a few channels this is ok. But now, if a single DSP will process say 30 channels (E1 worth), and there are say 24 DSP connected to the MCU, the MCU will not be able to handle this amount of traffic and it will become the system bottleneck. To eliminate this we open the door for distributed systems where the DSPs (8101's) using their CPMs will hook directly to the network and extract their own payload data directly from the network.~~

~~It is important to say that 8101 can be used both in centralized or distributed configurations!~~

~~I suggest you add the diagram here!~~

Compilability & Software Migration

One of the most productive new features of the MSC8101 is an exceptionally compilable architecture. The new chip's architecture was designed with extensive input from a team of leading compiler experts. Equipment designers and system developers can perform a much higher percentage of their programming in high-level languages (C and C++) than with prior DSPs. The resulting compiled code delivers such outstanding performance that it compares favorably with assembly code running on other DSPs. The compiled code also exhibits excellent code density.

Since time-to-market is a key customer requirement, the compilability of the MSC8101 allows customers to develop new systems faster and more cost effectively. Customers can also easily migrate code from other Motorola DSP architectures such as the 56300 family. Some of the program code created for applications in the 56300 series is written in high-level languages and only needs to be recompiled to run on the MSC8101 and future MSC810x chips.

Motorola is further supporting application and code migration to the MSC8101 by offering, in conjunction with third parties, a large library of ready-to-run application software. All such offerings will be optimized in C and/or hand-optimized in assembly language for the MSC810x series. Customers migrating to the MSC810x series from the 56300 family will also benefit from the substantial similarities in instruction architecture. Thus, customers who choose to optimize time-critical routines in assembly language will experience a faster learning curve.

The Star*Core Alliance, Motorola, and third party vendors are also offering a variety of support and development tools including: C/C++ compilers, an assembler, optimizer, linker, and simulator. Motorola is also offering two hardware tools, the MSC8101 evaluation modules (EVMs) and an application development system (ADS).

~~**Development Tools & Support**~~

~~Star*Core-based DSPs such as the MSC8101 offer a wide selection of best-in-class development tools. Customer design teams can select from multiple compilers, development environments, and real-time operating system software, to name a few.~~

~~The Star*Core Alliance offers baseline tools such as a C/C++ compiler, an assembler, optimizer, linker, and simulator. The compiler conforms to ANSI C and C++ standards and generates code that is exceptionally compact (comparable to assembly code running on other DSPs). The compiler maximizes and optimizes the parallelism available in the SC140 core and takes full advantage of the core's multiple execution units. The compiler also provides intrinsic support for ITU/ETSI primitives – useful for vocoder standard reference code. The compiler also supports source-level debugging when used with integrated development environments. These software tools are available in a complete visual integrated development environment (IDE), which also includes real-time source-level debugging and profiling tools.~~

~~An alternative C/C++ compiler is available from Green Hills Software, as part of its MULTI™ development environment. In addition, third-party suppliers Embedded Systems Products and ENEA OSE systems are offering real-time operating systems (the RTXC Operation System and the OSE Operating System, respectively).~~

~~Motorola will be offering a two different hardware tools. The MSC8101 evaluation modules (EVMs) and an application development system (ADS) for evaluating MSC8101 chips and debugging software are now available.~~

~~Motorola and its network of third-party partners are also developing a complete library of application software modules, optimized in C and hand-optimized where needed. Most of these modules will be provided when sample quantities of the MSC8101 become available. Included will be software for vocoders (such as standard CDMA, GSM, TDMA, and ITU vocoders), echo cancellation, fax, and modem functions.~~

Summary & Highlights

As the major paradigm shift from a digital to a Packetized world accelerates, equipment manufacturers will seek devices that deliver superior performance density at the lowest cost per instruction. Communications manufacturers are now working on ever shorter design cycle times ~~of as low as three months~~. DSP vendors must offer products that optimize equipment manufacturers' time-to-market and time-to-volume.

The new MSC8101 Digital Signal Processor is the industry's first DSP optimized for the Packetized world. It supports ATM, Fast-Ethernet, and fast TDM highways. The new device integrates the recently announced Star*Core 140 DSP Core with a CPM from the MPC8260 PowerQUICC II™. This qualifies it as the industry's first "network ready" DSP. The first PowerPC™ bus compatible DSP, the MSC8101 integrates the 64-/32-bit 60x PowerPC bus interface.

The MSC8101 uses the top of the line Power PC process technology, the HiPerMOS-6 with advanced copper interconnects, another industry first. The device features 0.13 micron geometries and a core operating speed of 300 MHz. Of great value to advanced communications infrastructure manufacturers, the device features very low power dissipation – 0.5W @ 1.5V for the whole device.

The combination of the highly advanced DSP architecture and the HiP-6 process technologies on the MSC8101 allows customers to leverage their device selection with proven Motorola IP (Intellectual Property). A few of the most popular IP selections available include the PowerPC bus interface, the MPC8260 Memory Controller and CPM, and the FSRAM memory cell which delivers 512KB of on-chip memory.

With a DSP on the inside and a PowerPC on the outside, customers gain the advantage of a commonality in their hardware design. System designers gain the ease of a glueless interface to integrate the PowerPC with the MSC8101. Customers can also reuse drivers and the MSC8101 can be used as a PowerPC companion processor.

The MSC8101 CPM is a programmable protocol machine that uses a 32-bit RISC engine. The CPM supports a wide variety of protocols, allows customers to reuse proven MPC8260 microcode, can incorporate customer specific protocols, and can be upgraded as future protocols emerge. The CPM provides network connectivity to standard backbones including 155 Mbps ATM SAR (Utopia bus) supporting AAL (0, 1, 2, and 5), 10/100 Mbps Ethernet, up to four E1/T1 interfaces or one E3/T3 and one E1/T1, and HDLC support up to T3 rates or 256 channels.